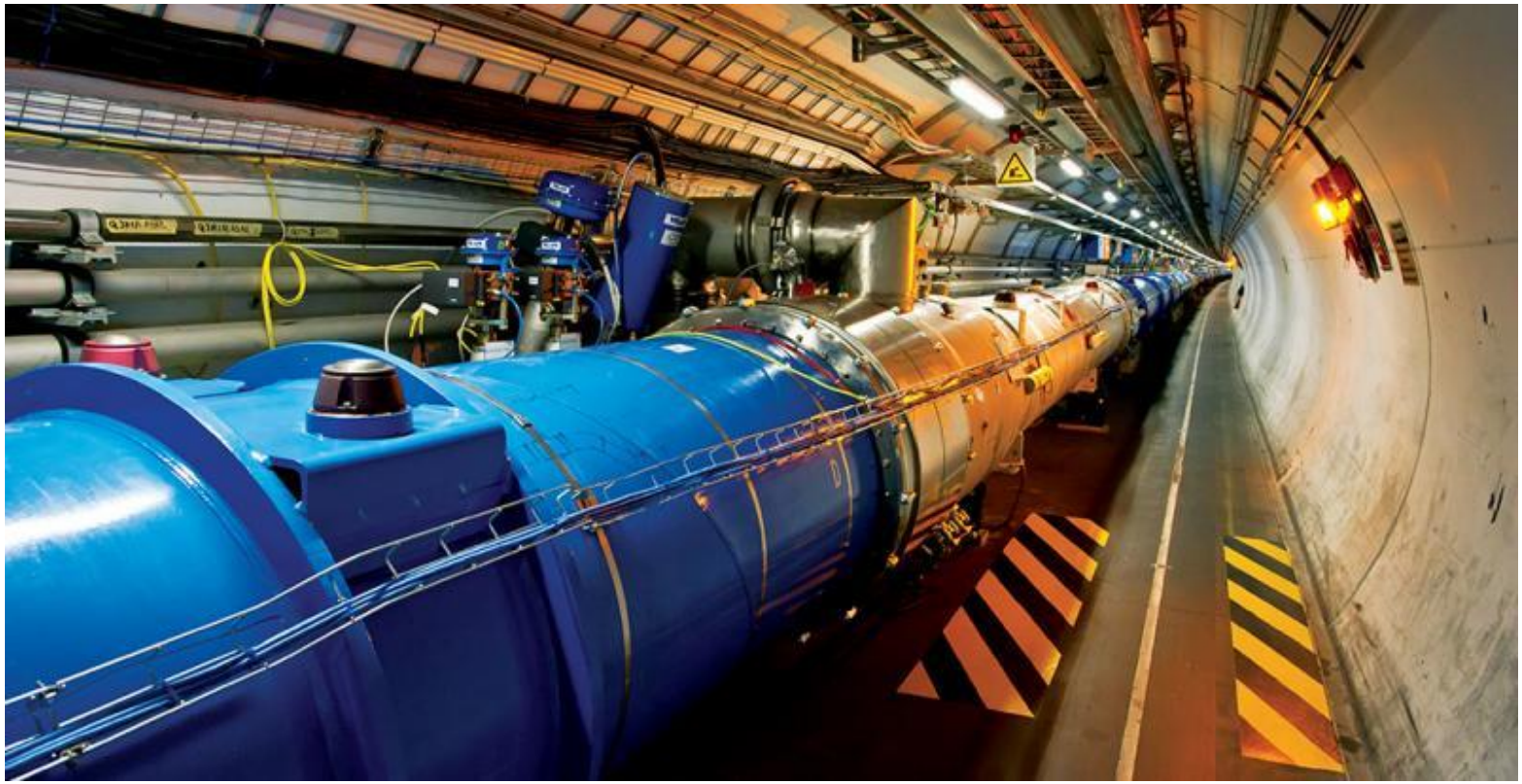

High DR ADC for LHC

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Last updated: 12/19/16

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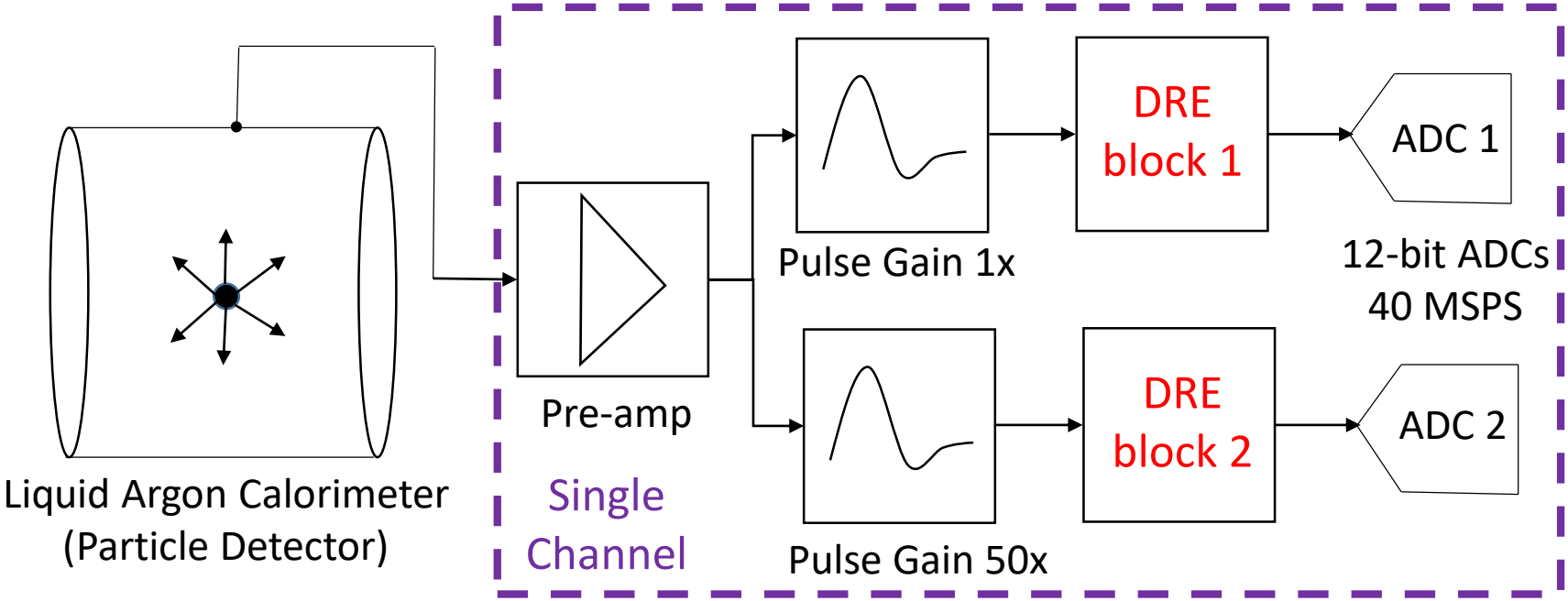
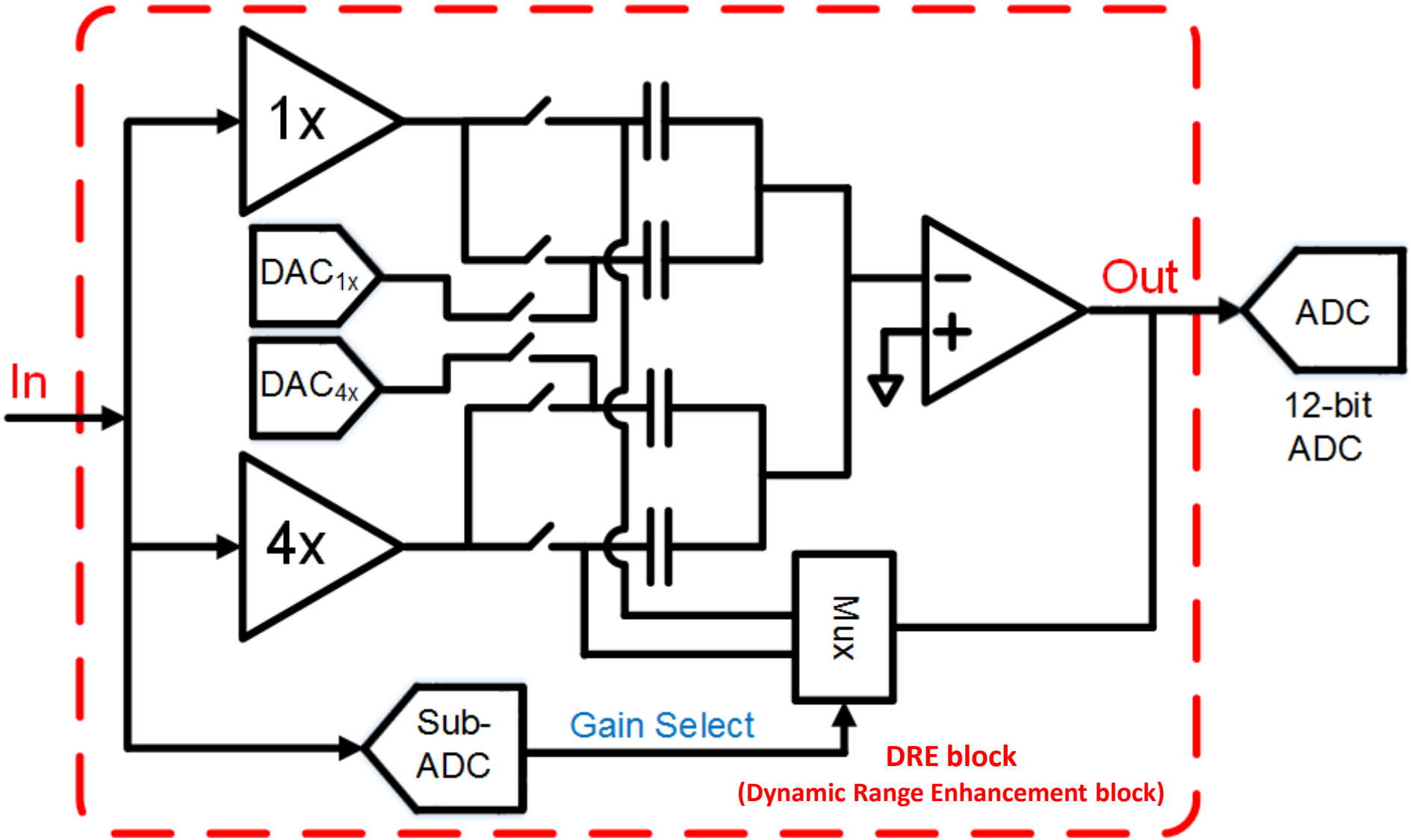
Aim: ADC design for The LHC (Large Hadron Collider), CERN

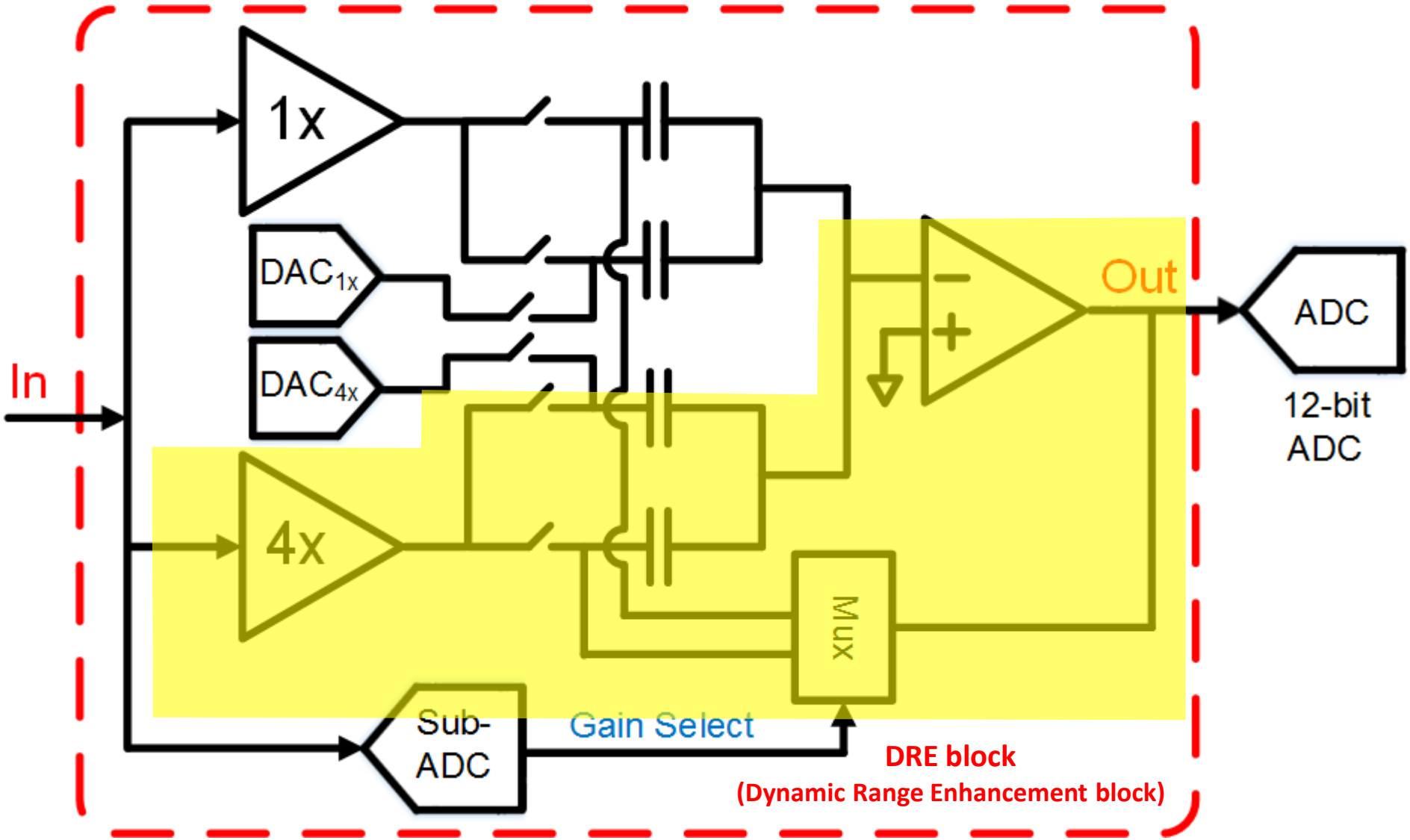
- ADC specifications:
  - 14-bit design: To accommodate high dynamic range (16 bit)
  - 40MSps
- To design: intermediate block
  - Increase accuracy to 14 bit (or enhance the dynamic range)



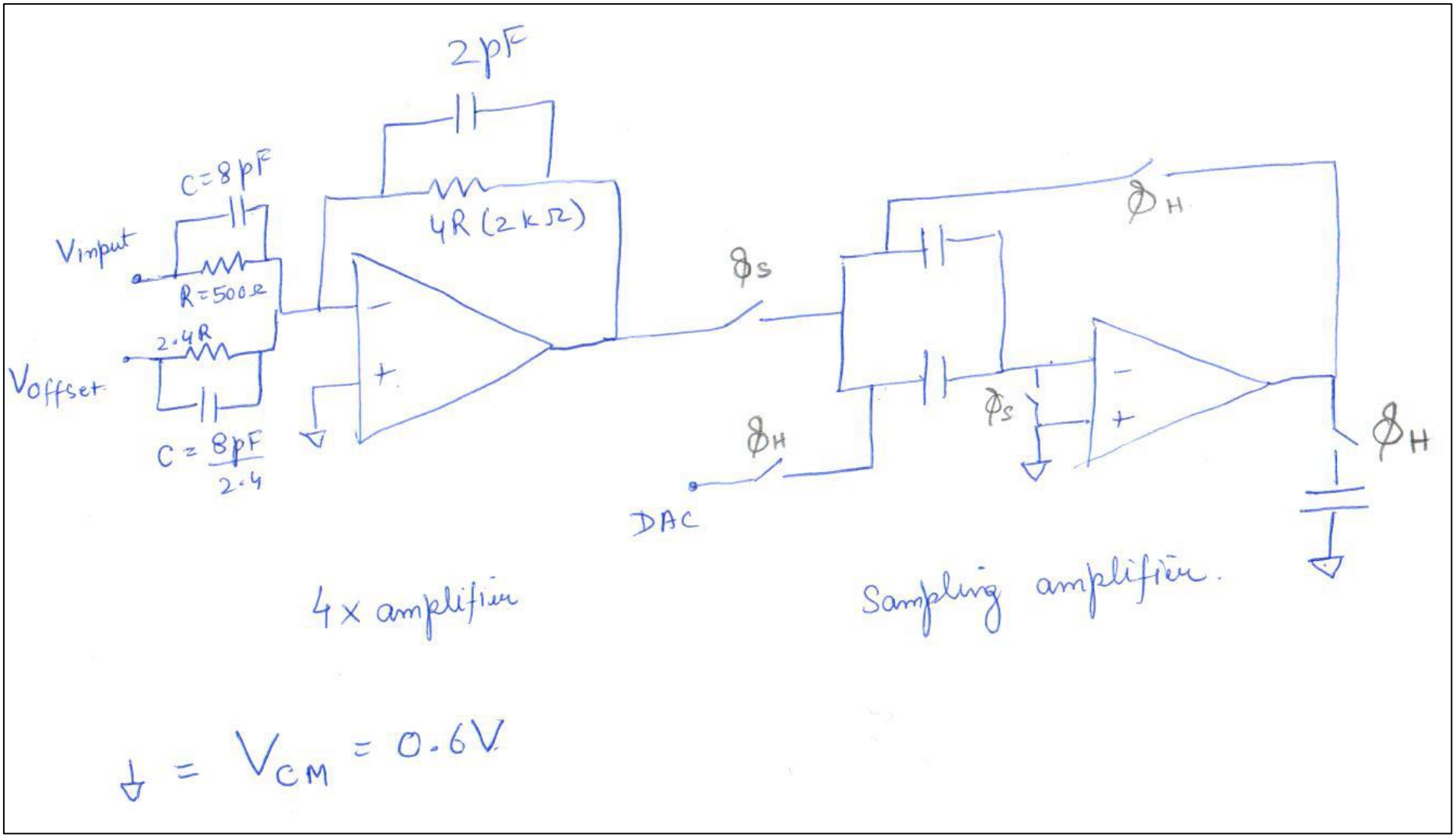
Proposed architecture: Concept



4x Branch simulation

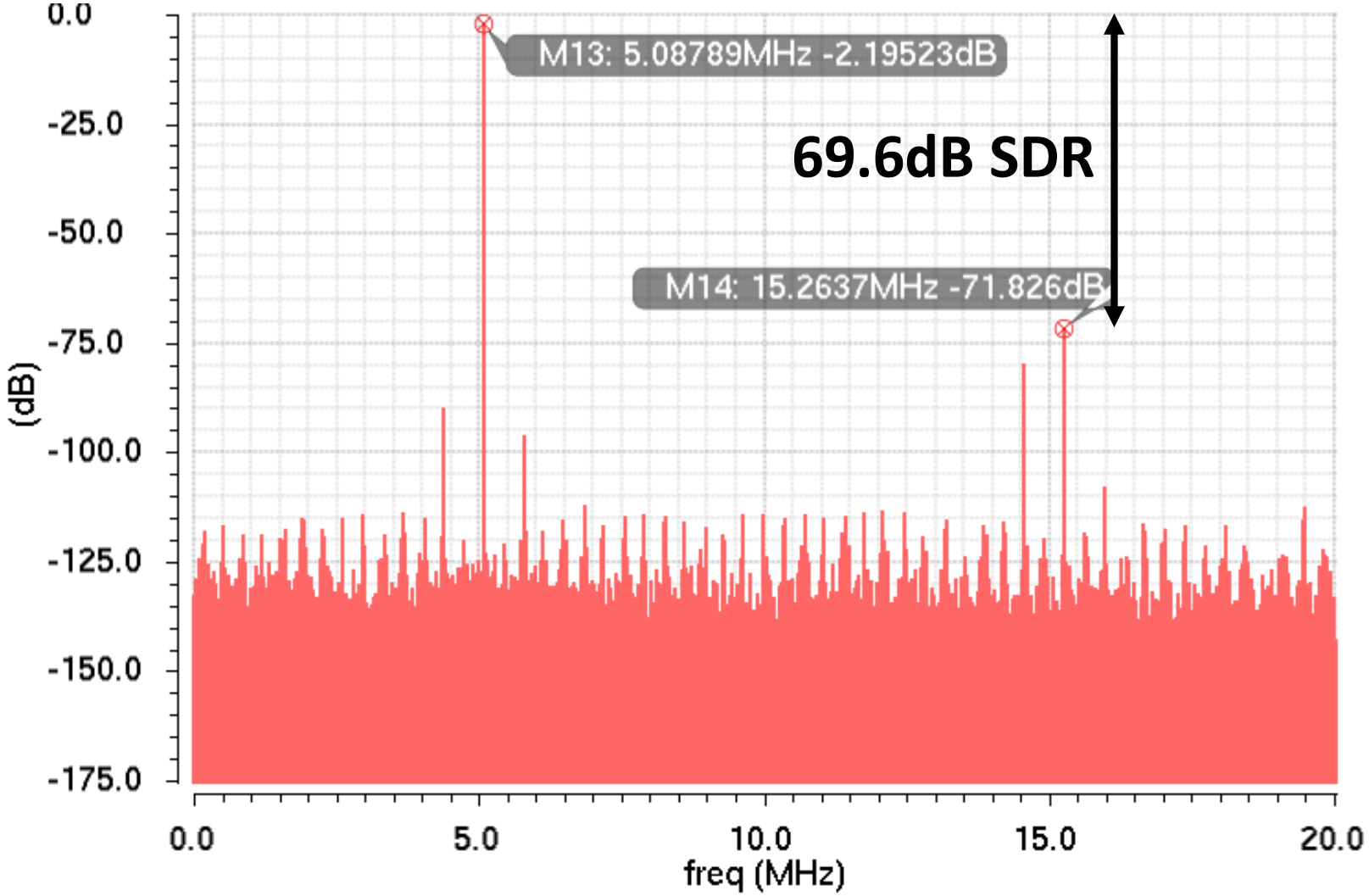


4x branch detailed schematic



Source impedance not implemented yet.

4x branch output fft for tt 0°C case



4x branch results summary @ 5MHz Input, 40MSPS

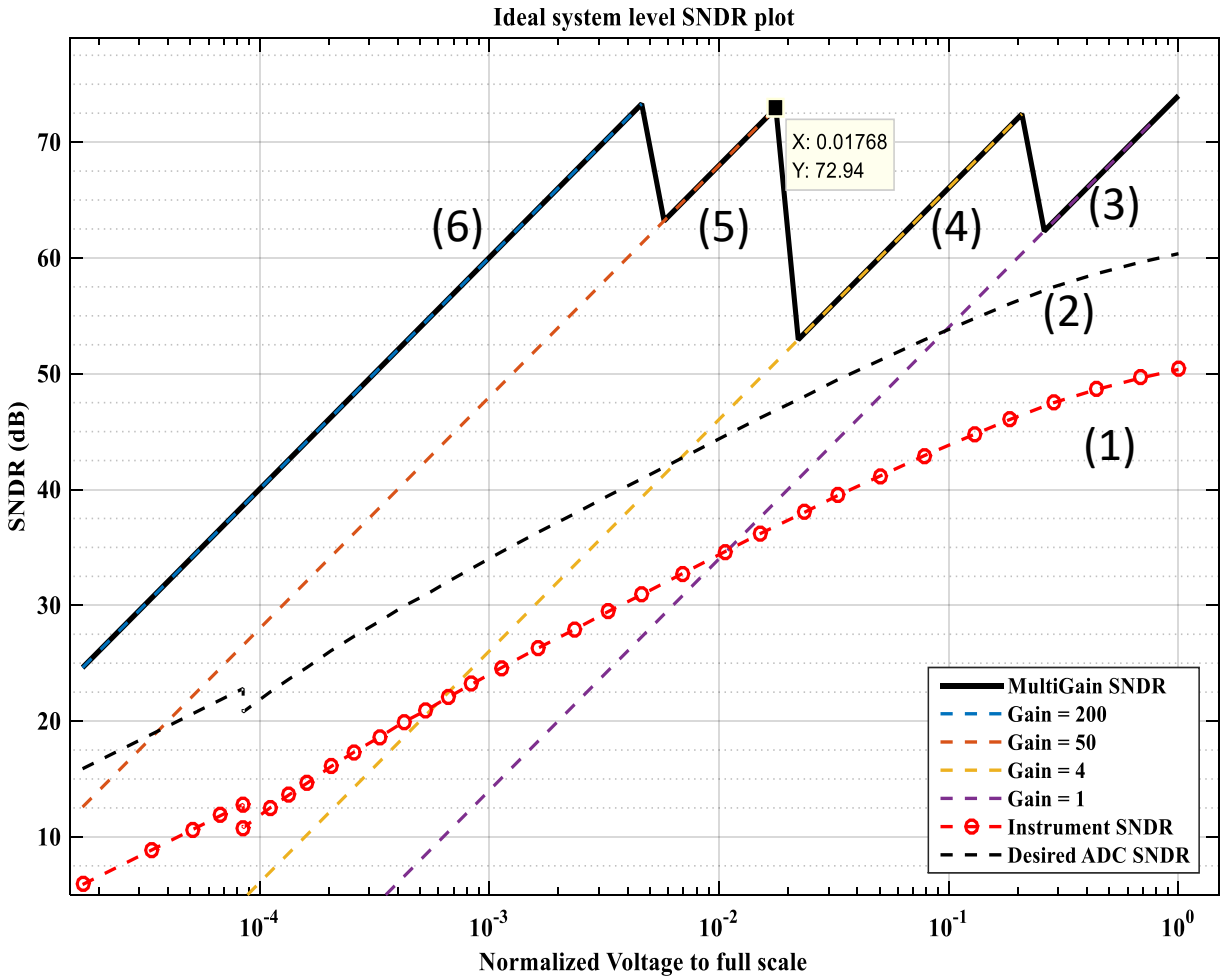
- Simulations contain:
  - Transistor level transient simulation
  - Transient noise enabled
- Tt, ff, ss, sf and fs corners simulated for 0°C and 50°C
  - Worst case (ss0) limited by both noise and distortion

Corner	SNR (dB)	SDR (dB)	SNDR (dB)	Power (mW)	$Vout_{pp}$ (diff) (V)
tt 0	63.0	68.5	62.0	108	1.6
tt 50	62.3	74.0	62.0	111	1.6
ss 0 (worst THD)	63.3	64.8	61.1	86	1.6
ff 50	62.4	82.7	62.4	121	1.6

System level SNDR requirements

- 1-bit provided by sample stage MDAC
- 11-bit ADC is expected to provide 67.7dB SNDR
- Overall 12-bit ADC requirement of 73dB obtained by combination of 1-bit output and 11-bit ADC

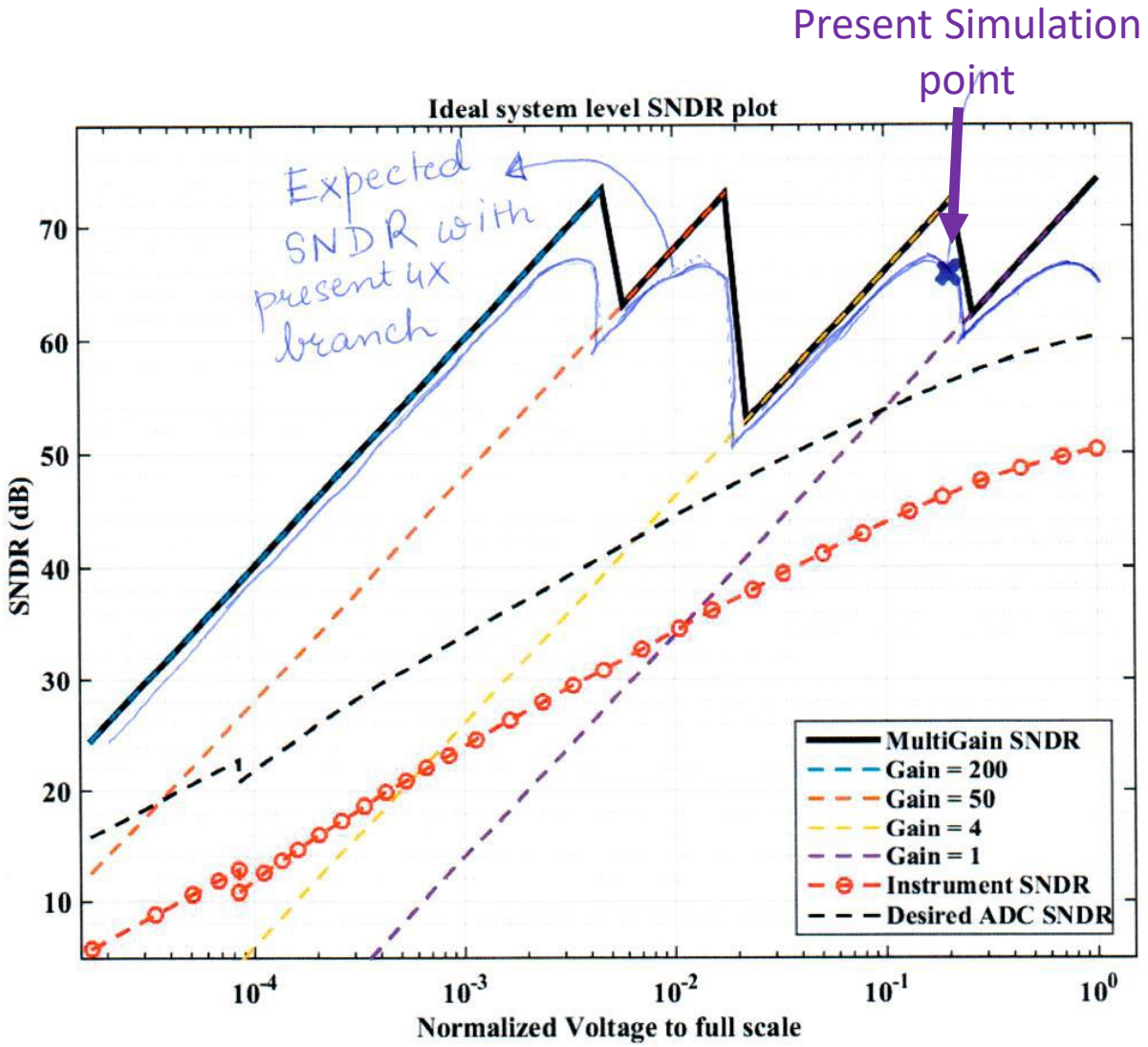
- Ideally need 67dB SNDR at the MDAC output.
- Currently worst case SNDR is 61dB.



System level requirements satisfied!

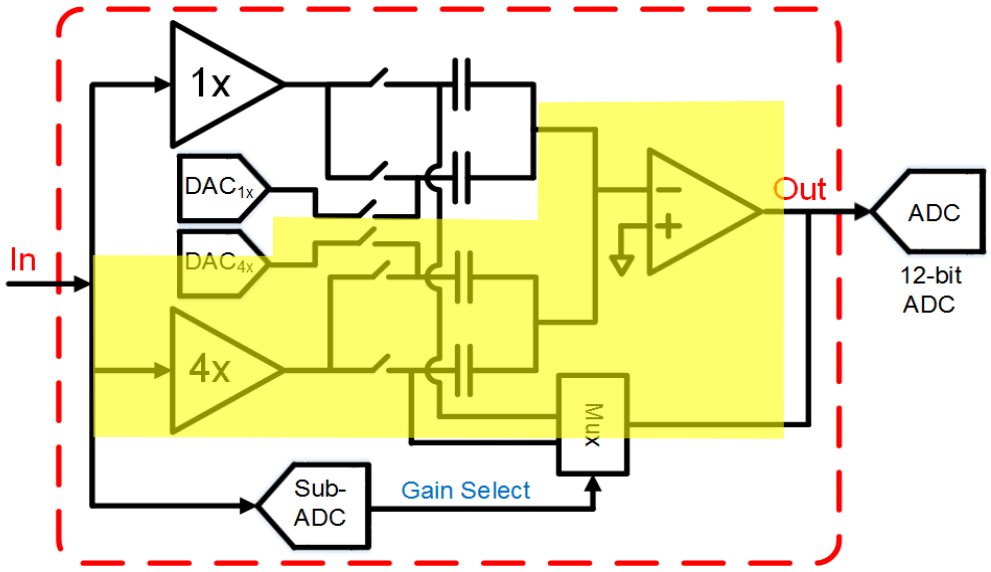
- 1-bit provided by sample stage MDAC
- 61.1 dB SNDR obtained in the worst case simulation
- After combining, SNDR obtained is 67.1dB

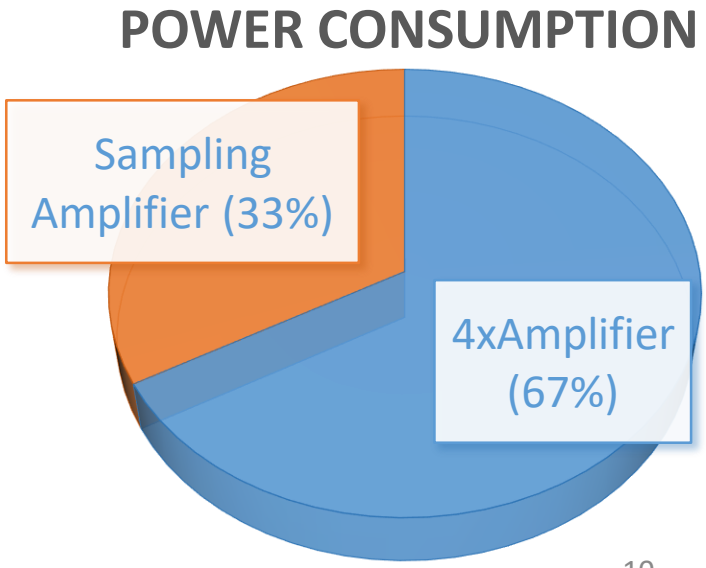
- Overall system level requirements are still satisfied



Power consumption for 4x branch

- For ss 0°C case:
  - Total power = 86mW
  - 4x Amplifier power = 58mW (67%)
  - Sampling Amplifier power = mW (33%)
- Power required in 4x Amplifier to increase SNR





DRE input requirements (1st Draft)

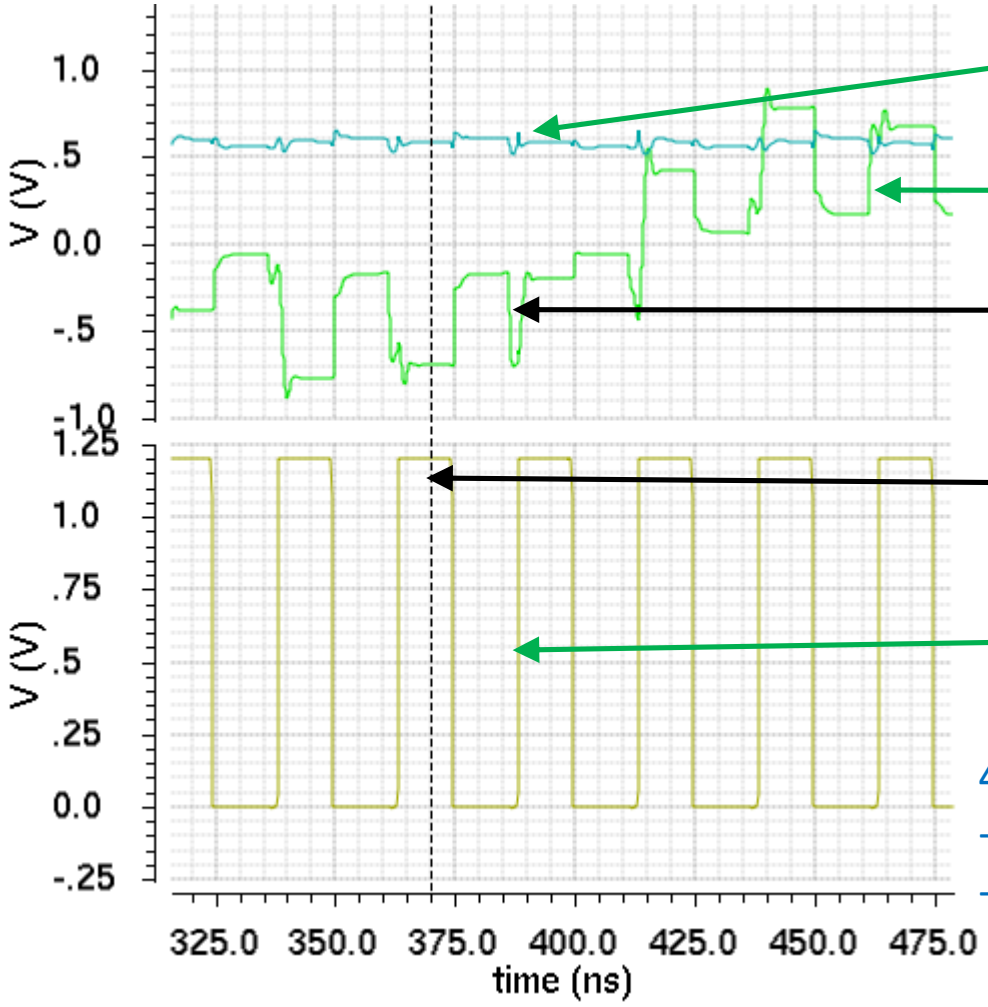
Requirement	Value
Input Resistance to be driven	250Ω single ended (1x and 4x branch having 500Ω each)
Input Capacitance to be driven	17pF Single ended (8pF each for 1x and 4x branch and 1pF for Sampling ADC)
Vpp differential input	1.6V

Future plans

- Verify dc shift for 4x amplifier branch.
- Implement 1x branch and verify.
- Combine 1x and 4x branch and simulate SNDR.
- Optimize individual components.

Backup slides

Sampled output waveform



Output Common Mode

Differential Output

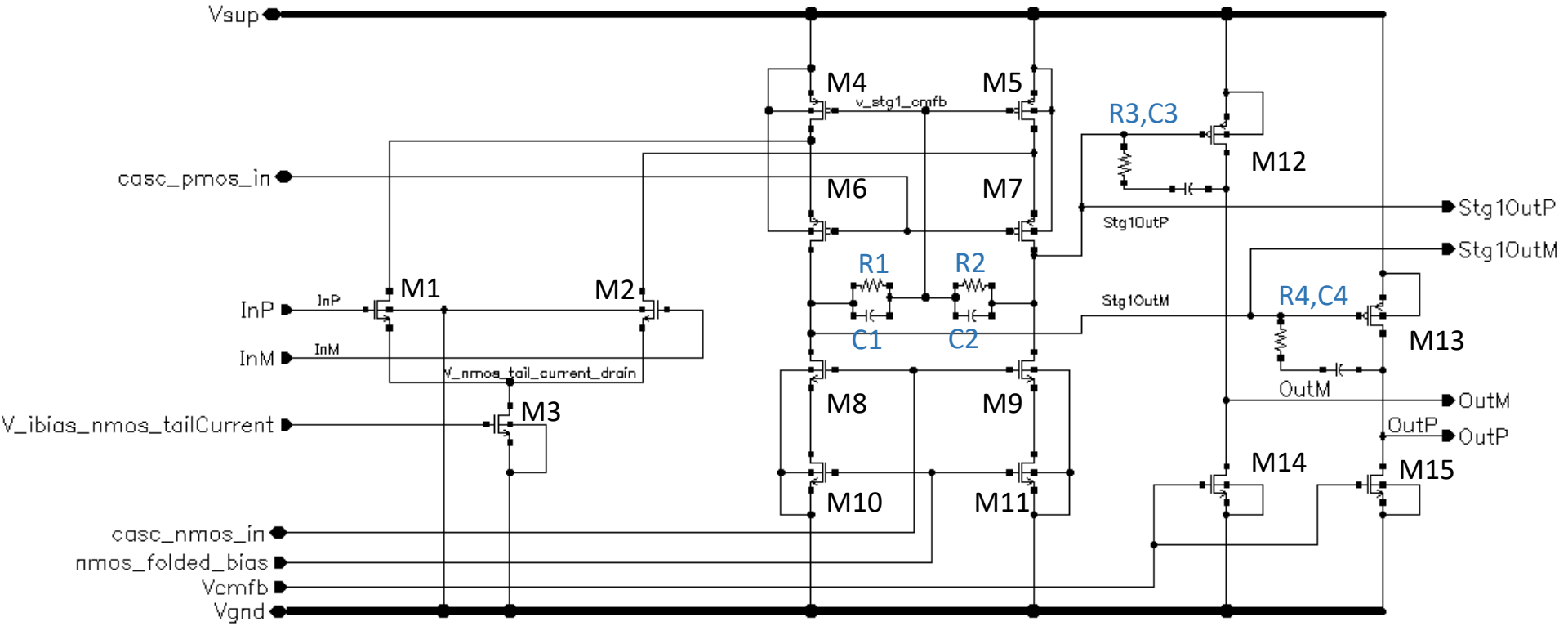
Sample and hold clock non-overlap period

Value settled by the end of hold clock

Hold clock

4x branch transistor level simulation for:
- 0.1V input amplitude (8x gain at output)
- tt 0°C case corner

4x Amplifier schematic



M1,M2 = 1920u/240n
M3 = 1280u/240n

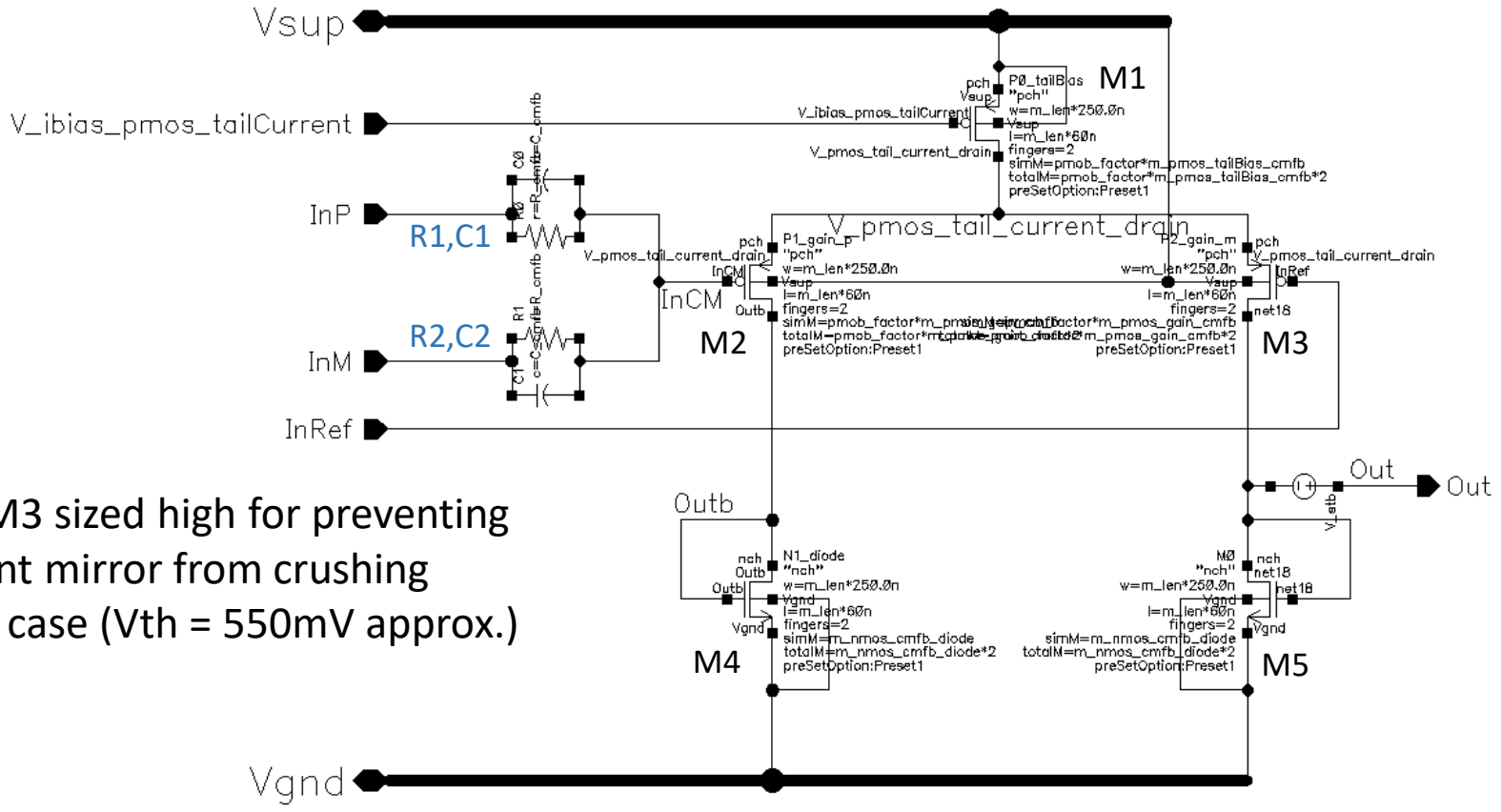
M4,M5 = 3840u/240n
M6, M7 = 5760u/240n
M8,M9 = 1920u/240n
M10, M11 = 640u/240n

M12,M13 = 1920u/240n
M14,M15 = 640u/240n

Cload = 4pF

R1,R2 = 200kΩ
R3,R4 = 0(zero)Ω
C1,C2 = 1pF
C3,C4 = 14pF

4x CMFB schematic



M2, M3 sized high for preventing current mirror from crushing for ss case (Vth = 550mV approx.)

M1 = 72u/240n
M2, M3 = 260u/240n
M4,M5 = 4u/240n

R1,R2 = 200kΩ
C1,C2 = 2pF

Amplifier sizing steps

- Started with 1mA current in each branch -> fixed W/L for tail current sources.
- Length = 4x chosen for getting better g_m/g_{ds} ratio
- For input transistor: Current mirror should not crush -> Higher W/L chosen (esp to account for ss case, with Vth = 550mV approx)
- Finally multiplicity of the amplifier was increased to 16x to achieve noise requirements for 4x amplifier.

1x branch: Can we eliminate amplifier?

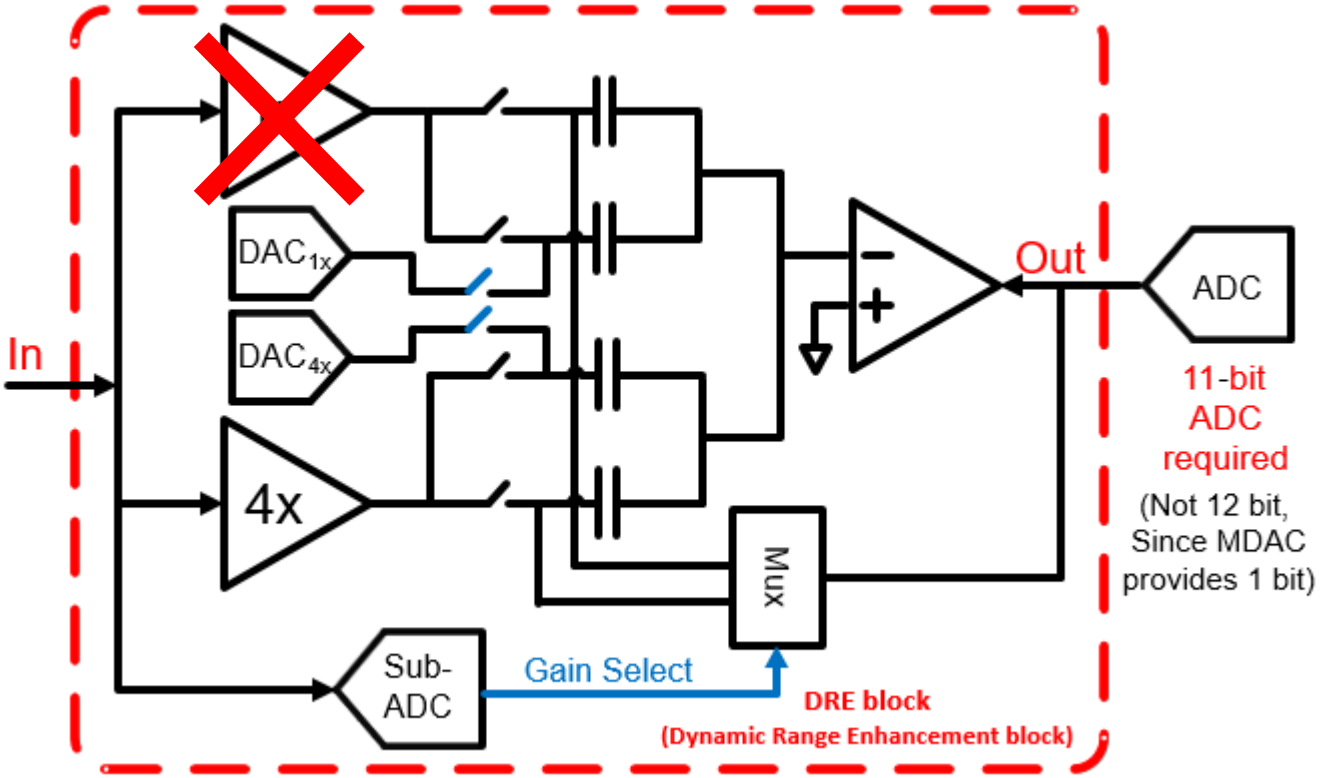
Why was 1x amplifier needed?

To equalize delays (4x and 1x branch)

How to eliminate?

Predict which branch to choose (1x or 4x) before 1st sample is chosen

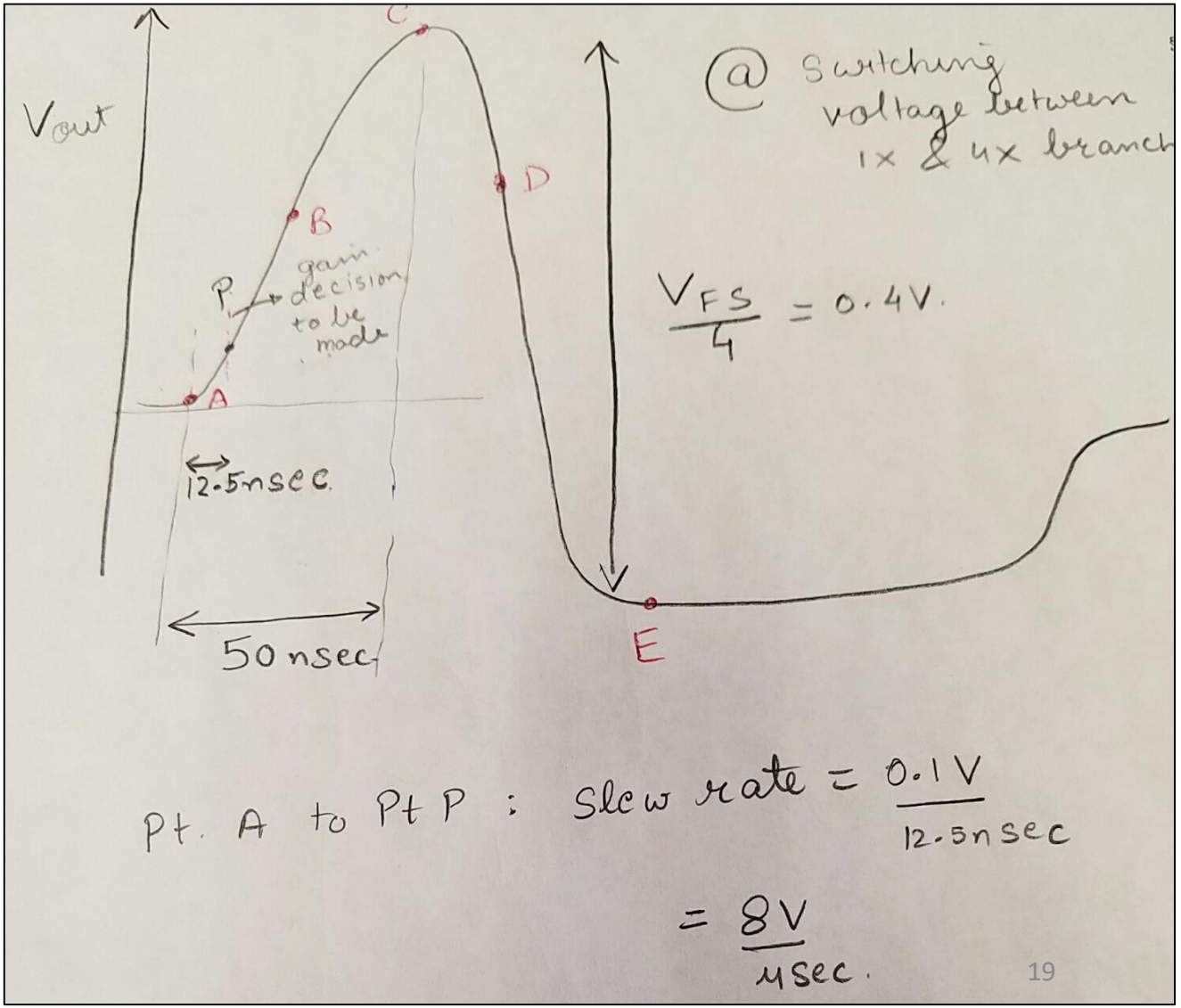
Benefit: Power savings



Waveform for V_{FS} / 4 input

- 4x vs 1x decision needs to be made by point P (12.5nsec) for sample at A.

- Choice:
  - Default = 1x gain.
  - Slew rate > 8V/µs -> Choose 1x gain for next 500nsec.



Possible architecture